REMARKS

Summary

Claims 1-41 were pending and all of the claims were rejected in the present office action. The Applicants have reviewed the cited art and the reasons given by the Examiner for the rejections and respectfully traverse these actions.

Claim Rejections

35 U.S.C. § 102 (e)

Claims 1, 2, 4-20, 25-29 and 35-37 were rejected under 35 U.S.C. § 102 (e) as being anticipated by Kay et al. (US 6,175,352; "Kay"). Of these, Claims 1, 25 and 32 are independent claims. The Applicants respectfully submit that a *prima facie* case of anticipation has not bee made out.

Claim 1 recites, *inter alia*, a first shift register, a second shift register having more stages than the first shift register, the stages of the second shift register are divided into groups, the stages of the first shift register are configured to transmit output pulse sequences having a predetermined number of consecutive pulses, and having different phases from each other to the stages constituting the groups of the second shift register as clock signals.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" Lindemann Machinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir 1984) (citing Connell v. Sears Roebuck & Co. 722 F.2d 1542 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

The Examiner asserts that "Kay teaches a shift register comprising: a first shift 21 register having a plurality of stages .... and a second shift register 12 having more stages than the first shift register... and stages of the first shift register...transmit output pulse sequences via switching elements 19_2 to 19_m...to the stages constituting groups of the second shift register...as clock signals φ_1 and φ_2...." (Office action, page 2).

The Applicants respectfully submit that, Kay teaches a second shift register 12 comprised of cascade-connected stages 13_1 to 13_n (col 3, lines 14-15), each stage being comprised of two memory devices, the second of each memory devices (e.g. 15_{m2}) having an output connected to a column addressing line. The second memory devices 15_{12} to 15_{m2} each have a clock input connected to a second line 17, φ2, of a bi-phase clock (col. 3, lines 22-24). Apart from the first memory device 15_{11}, all of the other first memory devices have their clock inputs obtained as the output of switching element 19, whose inputs are the first and second phases of the clock. The state of the switch is controlled by outputs of a first switch register 21, which controls the configuration of the switches 19_2 to 19_m (col. 3, lines 33-36). Depending on whether full or reduced display resolution is desired, the switch 19 is set to provide either a φ1 or φ2 clock signal to specified first memory devices of the shift register 12 (col.4, line 63, bridging col. 5 lines 3). When both memory devices of a stage are fed the same clock phase, the stage acts as a slave register, whereas stages being fed both phases act as master registers, so that the display resolution has been reduced by a factor of two, as the data is propagated to a master and a slave register essentially simultaneously (col. 5, lines 8-11) .

As taught by Kay (e.g., Fig. 1), at least one of the phases, φ2, is provided directly to the second memory device in each stage, and not by any output of the first register 21. Elements 19_2 to 19_m are single pole double throw switches whose state is statically controlled by outputs of shift register 21. The state of the switch is dependent on whether a full resolution or a reduced resolution is desired, and the resolution is not a dynamic property of a display. In any event, the φ1 clock signal is generated by the clock 18, and does not originate, nor is it modified by the shift register 21. Neither φ1 nor φ2 is supplied by the first shift register 21; the two clock phases are supplied by the clock 18 (col 4, lines 17-19).

Kay therefore teaches that the clock pulses are supplied to the second shift register 12 by a clock 18 , and not by the first shift register 21, which differs from the arrangement of Claim 1 where the stages of the first shift register are configured to transmit output pulse sequences, to the stages constituting the groups of the second shift register as clock signals.

Thus, the Examiner has not made out a *prima facie* case of anticipation, as not all of the elements of Claim 1 and their arrangement are found in the reference cited. As such Claim 1 is not anticipated, and is allowable.

Regarding Claim 25, the claim recites, *inter alia*, clock lines connected with the stages in each group, the clock lines configured to supply clock signals to the stages, the clock lines of each group isolated from the clock lines in each other group.

The Examiner has identified elements 13_1 through 13_m as groups of the second shift register 21. However the clock line for φ2 connects to each of the groups, and the connecting lines are connected to the same source, the clock 18. Hence, the clock lines for each group are not isolated, and Kay does not teach or suggest the arrangement of Claim 25,

Regarding Claim 32, recites, *inter alia*, isolating the clock lines between groups.

As discussed above, the clock lines in Kay are not isolated between groups, and thus Kay does not teach or suggest the arrangement of Claims 32.

For at least the reasons stated above, Claims 1, 25 and 32 are not anticipated, and are therefore allowable. Claims 2-24, 26-31 and 33-41 are claims dependent on one of the allowable independent claims and are allowable, without more.

35 U.S.C. § 103(a)

Claims 3, 21-24, 30, 31, 33, 34, and 38-41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kay in view of one of Tanaka (US 5,369,417; "Tanaka") and Ishii et al. (US 6,670,943; "Ishii"). Since Kay is used as the primary reference for each of the rejections, and the Applicants have shown that Kay cannot be depended on to teach all of the elements asserted by the Examiner, and none of the secondary references are cited to remedy this deficiency, the Examiner has not made out a *prima facie* case of obviousness against any of these claims. As such, the Applicants respectfully request that the rejection of Claims 3, 21-24, 31, 34 and 38-41 be withdrawn.

Conclusion

Claims 1-41 are pending.

For at least the reasons given above, the Applicants respectfully submit that the pending claims are allowable.

The Examiner is respectfully requested to contact the undersigned in the event that a telephone interview would expedite consideration of the application.

Respectfully submitted,

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